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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,596	01/27/2004	Baw-Ching Perng	TS02-405	3425

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,596	PERNG ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *15-38,41 and 42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14,39 and 40* is/are rejected.

7)☒ Claim(s) *12-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 02/23/2005.

Election/Restrictions

1. Applicant's election of species A, claims 1-14 and 39-40 in the reply filed on 02/23/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 15-38 and 41-42 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species.

Oath/Declaration

3. Oath/Declaration filed on 01/27/2004 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 39 is rejected under 35 U.S.C. 102(e) as being anticipated by Jin et al. [US 20030211748].

Jin et al. (figs 1-4 and text paragraphs [0001]-[0034]) discloses the claimed method comprising:

providing a substrate (wafer 114 including a doped layer 314, fig 3A, text paragraph [0032]);

depositing a high k dielectric layer (302, fig 3A, text paragraph [0032]) above said substrate;

forming a pattemed layer (306, fig 3A) above said high k dielectric layer; and

selectively etching exposed portions of said high k dielectric layer with a plasma etch comprising one or more halogen containing gases (fig 3A-3B, text paragraph [0032] & [0007]-[0008]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 7-11, 14 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. [US 2003/0211748] in view of Arai et al. [JP 2002-075972].

► With respect to claims 1, 4 and 14, Jin et al. (figs 1-4 and text paragraph [0001]-[0034]) discloses a method of removing a high k dielectric film comprising:

(a) providing a substrate (wafer 114 including a doped layer 314, fig 3A, text paragraph [0032]) ***[claim 1];***

(b) depositing a high k dielectric layer (302, fig 3A, col. 4 line 53) above said substrate wherein said high k dielectric layer has a thickness about 10 to 120 angstroms and is comprised of ZrO_2, HfO_2, Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3, La_2O_5 or is a silicate, nitride, or oxynitride of one or more of Zr, Hf, Ta, Ti, A1, Y, and La (e.g. 3 nm= 30 angstroms of high k dielectric, text paragraph [0032]-[0033] and [0016]) ***[claims 1 and 4];***

(c) forming a pattemed gate electrode (306, fig 3A) on said high k dielectric layer ***[claim 1]***; and

(d) anisotropically etching through exposed portions of said high k dielectric layer with a plasma etch comprising one or more halogen containing gases (fig 2-4, text paragraph [0032] & [0007]-[0008]: *the high k dielectric 302 in figure 3B shows vertical sidewalls after being etched by the plasma etching step 216 due to anisotropic etch characteristics of the etching step 216*) wherein the etch rate of said high k dielectric layer in step (d) is more than twice the rate of etching silicon oxide or silicon ***[claims 1 and 14].***

Jin et al does not expressly teaches said substrate being provided with isolation regions and an active area between said isolation regions ***[claim 1]*** wherein the substrate is silicon and the isolation regions are comprised of silicon oxide ***[claim 14]***.

However, providing the substrate of silicon with the isolation regions of silicon oxide and the active area between the isolation regions has been known in the art. See

Arai et al. as an evidence that shows the substrate (1, silicon) being provided with the isolation regions (3, silicon oxide) to define the active region there between for forming the transistor including high-k gate dielectric and gate electrode.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, to modify process of Jin et al. by using the substrate including the isolation regions and active area as being claimed, per taught by Arai et al., to define the region for forming transistors as being needed in a semiconductor device.

► With respect to claim 5, ALD, CVD and MOCVD are known techniques for depositing high k dielectric layer. See Arai et al. (text paragraph [0031]) as an evidence that shows depositing the high k dielectric (4) by CVD. Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Arai et al, to select the known technique of deposition as being claimed in the process of Jin et al to form the high k dielectric for improving performance the transistor of semiconductor device.

► With respect to claims 3-4, Jin et al. (fig 3A, text paragraph [0032]) shows forming an interfacial layer (304) comprised of silicon oxide, silicon nitride or silicon oxynitride (silicon dioxide) with a thickness between about 1 and 30 angstrom (20nm = 20 angstroms) prior to depositing the high k dielectric layer (302).

► With respect to claim 7, Jin et al. (text paragraph [0016]) discloses wherein said one or more halogen containing gases comprises CF_4, CHF_3, CH_2F_2, BCl_3, Br_2, HF, HCl, HBr, HI, NF_3 and mixtures thereof (e.g. HCl).

► With respect to claims 8-11, Jin et al. (text paragraph [0016] & [0007]-[0008]) further discloses adding one or more of 0_2, CO, CO_2, and N_2O as an oxidant gas and adding one or more inert gases including Ar, Xe, He and N_2 in step (d). The claimed ranges parameters for anisotropically etching the high k dielectric are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955)., the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

► With respect to claim 40, Jin et al substantially discloses the claimed method including configuring the patterned layer (306, fig 3A, *text paragraph [0033]*) to be a

patterned gate electrode on said high k dielectric layer (302) and carrying said selectively etching in a manner that including anisotropically etching through said high k dielectric layer with said plasma etch *(fig 2-4,* text paragraphs [0016]-[0033]*:* the high k dielectric 302 in figure 3B shows vertical sidewalls after being etched by the plasma etching step 216 due to anisotropic etch characteristics of the etching step 216*)*.

Jin et al does not expressly teaches said substrate being provided with isolation regions and an active area between said isolation regions.

However, providing the substrate with the isolation regions and the active area between the isolation regions has been known in the art. See Arai et al. as an evidence that shows the substrate (1, silicon) being provided with the isolation regions (3, silicon oxide) to define the active region there between for forming the transistor including high-k gate dielectric and gate electrode.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, to modify process of Jin et al. by using the substrate including the isolation regions and active area as being claimed, per taught by Arai et al., to define the region for forming transistors as being needed in a semiconductor device.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. [US 2003/0211748] in view of Arai et al. [JP 2002-075972] as applied to claim 1 above, and further in view of Ahn et al. [US 2004/0038554].

With respect to claim 6, ZrO_2 or HfO_2, including one of Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3, La_2O_5 as a minor component are known material of high k dielectric that are used for forming semiconductor device. Selection of a known material based on its suitability for

its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301. See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious).

In addition, Ahn et al. as an evidence shows that using HfO_2 including Ta_2O_5 as a minor component for high k dielectric will improve characteristics of thermal stable for gate dielectric of transistor.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process Jin et al in view of Arai et al by using the high k dielectric as being claimed, per taught by Ahn et al., to provide a better transistor with a better thermal stable high k gate dielectric.

Allowable Subject Matter

7. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following are statements of reasons for the indication of allowable subject matter:

► Recorded Prior Art fails to disclose or suggest the combination of the process steps as recited in the base claim 10 including wherein a high k dielectric layer

comprising HfO_2 is etched by a method that includes a CF_4 flow rate of about 30 sccm, a CH_3F flow rate of about 60 sccm, an 0_2 flow rate of about 10 sccm, a 5 mtorr chamber pressure, RF power of about 600 Watts and a bias power of about 200 Watts for a period of about 10 seconds as characteristics in claim 12.

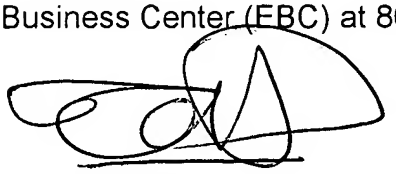
► Recorded Prior Art fails to disclose or suggest the combination of the process steps as recited in the base claim 11 including wherein a high k dielectric layer comprising HfO_2 is etched by a method that includes a CF_4 flow rate of about 5 sccm, an 0_2 flow rate of about 200 sccm, an Ar flow rate of about 100 sccm with a chamber pressure of 20 mtorr, a RF power of about 600 Watts, and a bias power of about 100 Watts for a period of about 23 seconds to end point plus an overetch period for about an additional 23 seconds beyond end point as characteristics in claim 13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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